AIR BRIDGE BASED PLANAR HYBRID TECHNOLOGY FOR MICROWAVE AND MILLIMETERWAVE APPLICATIONS

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ABSTRACT

A new silicon based, planar hybrid technology is being developed to address limitations associated with packaging and interconnections. The approach combines the advantages of both hybrid and monolithic technologies. Microwave transistor chips (GaAs FETs) are integrated in high resistivity silicon substrates with a vertical precision of better than 2 μm and lateral tolerances less than 10 μm. Air bridge technology and thin film techniques are then used to provide the necessary interconnections. The basic features of the proposed technology are presented here.

INTRODUCTION

Packaging and interconnections are increasingly becoming the limiting factors in system performance. The availability of low-cost and reproducible microwave and millimeterwave circuits is of great importance to systems in the future. A promising way to meet these requirements are integrated circuits based on silicon substrate [2], [10], [13]. Microwave devices such as FETs which are suitable for applications in this frequency range are, however, based on GaAs because of its superior electrical performance. Consequently, GaAs based device technologies, e.g. for MESFETs and HEMTs, are well developed. Commercial HEMT chips covering frequencies beyond 60 GHz are available [9]. Generally, hybrid technologies have therefore been used for many different applications as a good compromise between cost and performance e.g. [1], [3].

In the classical hybrid integration approach, active devices are mounted on top of the substrate and the interconnections are made by bonding wires. Such interconnections are not reproducible and at microwave frequencies exhibit undesirable parasitic inductances which degrade and limit the circuit performance and bandwidth respectively. A technology that circumvents these limitations is Flip Chip bonding [1], [8], [14]. Devices are manufactured with suitable bonding pads leading to very short and reproducible interconnections. However, a large number of microwave devices, either low-noise or low-power do not have bump contacts and must be bonded [3]. Planar interconnect technologies focusing specifically on low-power microwave devices have been reported [5], [6]. The proposed technologies also require very short interconnections which, however, must be carried out in a bonding step.

This paper presents a novel hybrid technology whereby GaAs FET devices are integrated in a silicon substrate in a planar position and interconnections made by employing air bridge technology as in monolithic circuits. The approach takes advantage of the conventional silicon micromachining technology, thin film technology

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and, as active devices, commercially available GaAs FETs in chip form. The high resistivity silicon substrate serves as a basis for realizing distributed passive coplanar components.

THE NEW TECHNOLOGY APPROACH

The proposed technology is based on two main steps, namely planar integration of the GaAs FETs in Si substrate and thin film/air bridge interconnections of the embedded chip to the rest of the circuit.

a) Planar Embedding Technique

This is the first and most important technological step. The aim here is to make an opening in a substrate and then glue an active device in it such that a plane surface between the active device and substrate results. This must be attained to guarantee for the successful subsequent processing associated with lithography and metallisation.

Two possibilities, wet etching or dry etching, exist for micromachining of silicon. Dry etching with inductively coupled plasma and cryo-temperature of the substrate allows the etching of grooves with vertical sidewalls and etching rates up to 2 to 4 μm/min (Fig.1) [12]. Although the cross-sectional dimensions of an opening for a chip can be exactly defined, the etching depth is difficult to control without laser interferometry. Wet etching of silicon (with <100> crystal orientation) results in slanting sidewalls. The resulting gap between a mounted chip and silicon is impossible to planarize [15]. A technique based on wet etching of openings in Si and using a planarization adhesive film was therefore developed.

Fig. 2 shows a summary of the procedure developed for high precision mounting of chips in a substrate. A silicon substrate is etched in KOH solution at the required opening positions. Next, an adhesive film is spanned with care to cover the opening. A chip is then introduced face down into the substrate and positioned on the adhesive film. The gaps between the chip and the substrate are filled out with an epoxy resin (Epo-Tek H77-S) or polyimide. After the glue dries up, the adhesive film is pulled away leaving a plane surface. A surface planarity of less than 2 μm has been achieved. A scan of the surface profile across an embedded chip and the surrounding substrate area is shown in fig. 3. A typical low-noise microwave transistor chip has dimensions of the order 350x400x100 μm which calls for very fine handling. Although similar techniques have been proposed for multi chip modules in general [4], [7], [11], they have not yet been investigated for microwave applications.

b) Interconnection Technology

The interconnections to the embedded active device are realized by using air bridge technology. This technology offers low parasitic interconnect capacitance and low inductance. Furthermore, this technique eliminates uncertainty that may be caused by the small non-planarity of the surface. A cheaper technology based on aluminium rather than standard gold plated bridges has been developed. Fig. 4 depicts a schematic diagram of this air bridge fabrication technique. The use of aluminium though not mandatory allows a further option to re-use accurately characterized low-power devices in final circuit fabrication. If the basic circuit is to be fabricated using gold metallization, the aluminium air-bridge interconnections on the micro-test-fixture [15] can be selectively etched away allowing the final circuit and new interconnections to be fabricated.

First a thick layer of photoresist is spun on the substrate and patterned. After a careful bake of the resist for removing all solvents a 2 μm thick aluminium layer is evaporated under rotating/swaying motion of the substrate for uniform covering of the resist slopes/edges. Then a second layer of photoresist is spun on and patterned. The extra aluminium is etched away and finally the resist is stripped leaving stable air bridges. Fig. 5 shows scanning electron micrographs of test air bridges. The aluminium thickness is 2 μm and the headroom width is 6μm.

A silicon micro-test-fixture based on a preliminary version of this technology using bondwires instead of airb-bridges was presented elsewhere [15]. A number of low-power microwave circuits are still under investigation and a comprehensive analysis of the results will be presented at a later date.

CONCLUSIONS

A low-cost hybrid technology for microwave circuits has been described. GaAs FET devices have been integrated in a quasi-monolithic manner in silicon substrates. Planar, very short and reproducible interconnections complete the simple assembly with promising microwave performances at low-cost.

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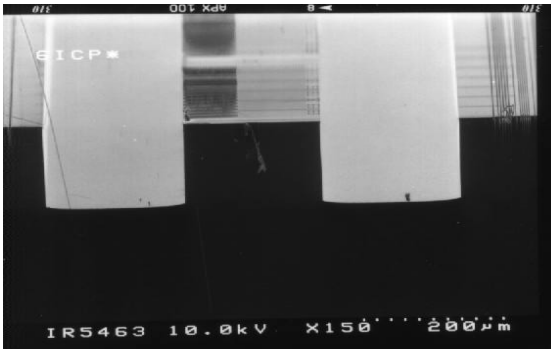

Fig. 1: Cross-section of grooves etched with SF_6/O_2 plasma at a substrate temperature of -100°C.

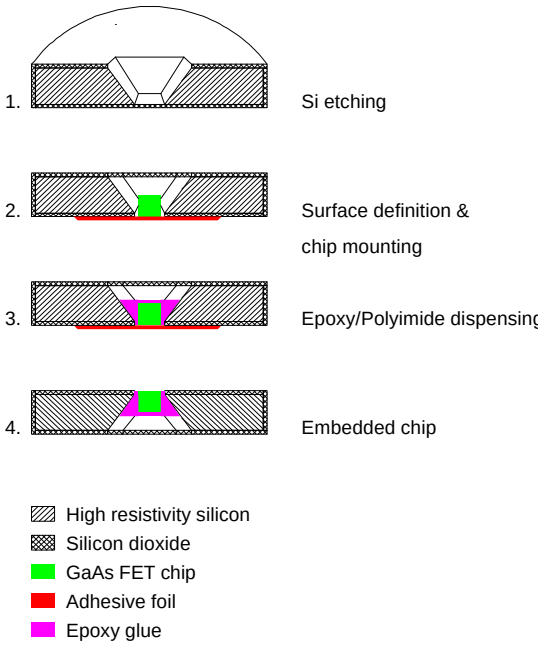

Fig. 2: Procedure for high precision integration of GaAs FETs in Si substrate.

Fig. 3: (a) Top view of GaAs PHEMT chip mounted in a Si Substrate.

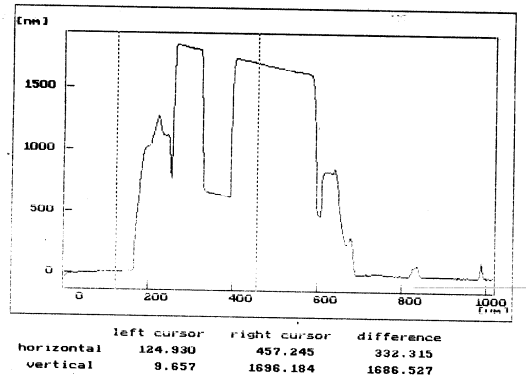

Fig. 3: (b) Profilometer scan of the chip in (a)

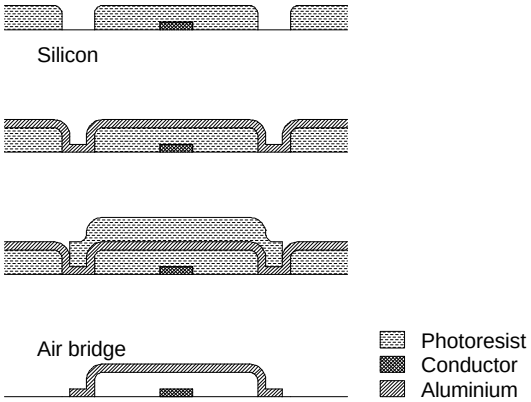

Fig.4: Fabrication steps for the air bridges.

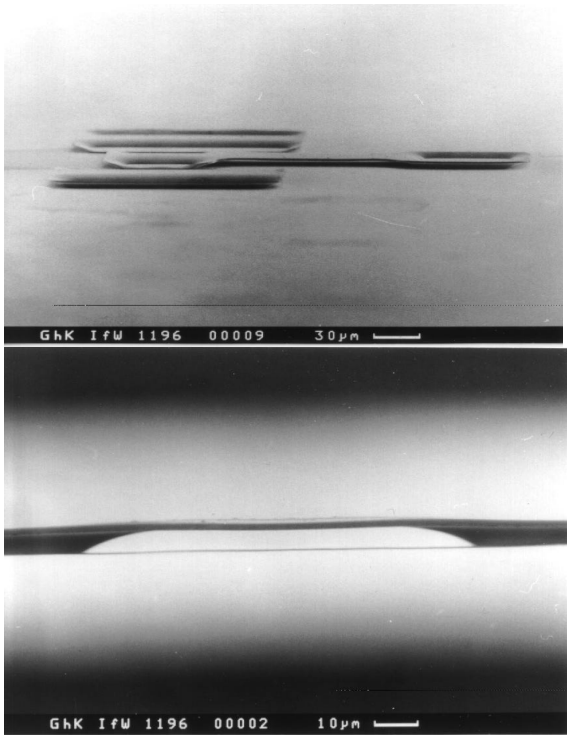

Fig. 5: Scanning Electron Micrographs (SEM) of test air bridges.